REMARKS

Claims 1-19 are currently pending in the subject application and are presently under consideration. Favorable consideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1-19 Under 35 U.S.C. §103(a)

Claims 1-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Schmidt *et al.* (US 5,212,631) in view of Sharma *et al.* (US 6,085,263). Withdrawal of this rejection is respectfully requested for at least the following reasons. Schmidt *et al.* and Sharma *et al.*, either alone or in combination, fail to teach or suggest all the limitations embodied in the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations.*** *See* MPEP §706.02(j). The ***teaching or suggestion to make the claimed combination*** and the reasonable expectation of success ***must be found in the prior art and not based on the Applicant's disclosure.*** *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The claimed invention relates to a system and method for I/O forcing using an I/O processor having a cache memory, wherein a processor and an I/O processor are operatively coupled to shared memory. Independent claim 1 recites *an I/O processor for performing at least one of input and output functions, the I/O processor and the processor operatively coupled to the shared memory, the* ***I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values stored in the shared memory, the I/O processor storing input values in the shared memory based at least in part upon forced I/O values stored in the cache memory,*** *the I/O processor*

determining output values based at least in part upon forced I/O values stored in the cache memory. Independent claims 6 and 9 recite similar limitations. It is apparent therefore, that the invention as claimed comprises in part, an I/O processor that performs input and output functions, wherein the I/O processor is operatively coupled to shared memory. The I/O processor is further operatively coupled to a cache memory, the cache memory storing a portion of the forced I/O values that are also stored in the shared memory. The I/O processor further stores input values in shared memory based at least in part on a determination of the forced I/O values that are stored in the cache memory. The I/O processor in addition, determines output values that are to be utilized based at least upon forced I/O values stored in cache memory. Both Schmidt *et al.* and Sharma *et al.*, either alone or in combination, fail to teach or suggest these novel features of the invention as claimed.

As the Examiner concedes in the Final Office Action dated February 24, 2004, Schmidt *et al.* is silent regarding an: "I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values stored in shared memory ... storing input values in the shared memory and determining output values based at least in part upon forced I/O values stored in the cache memory." *Id.* at page 3. Applicants' representative further asserts that in addition to the deficiencies identified by the Examiner, Schmidt *et al.* fails to teach or suggest the limitation that the I/O processor determines whether or not to store input values in the shared memory ***based at least in part upon forced I/O values stored in the cache memory***. In order to rectify the acknowledged deficiencies, the Examiner attempts to rely upon Sharma *et al.* to make up for that which Schmidt *et al.* fails to teach or suggest.

Sharma *et al.* discloses an I/O processor (IOP) for delivering high I/O performance while maintaining inter-reference ordering among memory reference operations issued by an I/O device as specified by a consistency model in a shared memory multiprocessor system. The Examiner asserts that Sharma *et al.* discloses an I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values in the shared memory, at col. 14, lines 9-37, which discloses an IOP that comprises:

> ... a plurality of input request queues, each of which interface to the I/O bus to receive memory reference operations issued by an I/O device and loaded into a tail of the queue. To maintain order of the issued memory references, all operations from a particular I/O device are preferably loaded into a particular one of the input request queues. A head of each input request queue is coupled to the prefetch controller. As described herein, the prefetch controller examines the address of each memory reference operation at the queue head and compares it with addresses stored in the cache entries. The controller is also coupled to an output request queue and a retire queue. Operations pending in the output request queue are eventually sent to the system over the switch.
>
> Based on the results of the comparison operation, the prefetch controller either enqueues (loads) a prefetch request into the output request queue while loading the operation into the retire queue or it loads the memory operation solely into the retire queue. The decision is based on whether the data pertaining to the operation is stored in the cache or if it has already been prefetched; if it is, indicating the prefetching is not required, the controller loads the operation into the retire queue without issuing a prefetch request to queue. It the prefetch controller discovers that the data for the operation must be prefetched, it copies the operation into the retire queue and loads a prefetch request (i.e., a Rd or RdMod request) into the output request queue. (reference numerals omitted).

Nowhere in the foregoing cited passage is mention made of an I/O processor coupled to a cache memory ***storing at least a portion of the forced I/O values in shared memory***. Rather, Sharma *et al.* at best discloses a *prefetch controller* that is coupled to a cache memory; the *prefetch controller* utilizing a cache memory to compare memory references at the head of an input queue with memory addresses stored in the cache memory. In fact, Sharma *et al.* fails to even teach or suggest utilizing a shared memory to store forced I/O values, let alone storing a portion of the forced I/O values stored in shared memory into cache memory. Thus, the invention as claimed is clearly distinguishable from both Schmidt *et al.* and Sharma *et al.*, as neither teach nor suggest, either alone or in combination, each and every limitation set forth in the subject claims. Accordingly, it is respectfully requested that the rejection of independent claims 1, 6 and 9, and associated dependent claims, should be withdrawn.

With respect to independent claims 10 and 17. Independent claims 10 and 17 recite similar claim limitations: ***forcing the input or output based at least in part upon***

the forcing information loaded in the cache. As the Examiner acknowledges in the Final Office Action dated February 24, 2004, Schmidt *et al.* fails to teach or suggest "loading a cache with forcing information associated with a forced input or output and forcing the input and output based at least in part upon the forcing information loaded in the cache." *Id.* at page 4. Thus, the Examiner attempts to utilize Sharma *et al.* to rectify this deficiency, and refers applicants' representative to col. 14, lines 9-37.

Sharma *et al.* at the indicated passage, however, aside from utilizing a cache memory to compare whether or not memory references at the head of an input queue are stored within the cache memory, fails to teach or suggest utilizing the information contained within the cache to ***force input or output.*** No mention whatsoever is made within Sharma *et al.* of this novel facility. Accordingly, withdrawal of this rejection with respect to independent claims 10 and 17, and claims that depend therefrom, is respectfully requested.

CONCLUSION

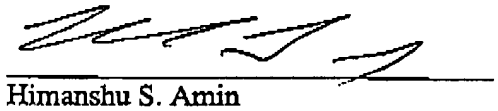
The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

AMIN & TUROCY, LLP



Himanshu S. Amin
Reg. No. 40,894

AMIN & TUROCY, LLP
24TH Floor, National City Center
1900 E. 9TH Street
Cleveland, Ohio 44114
Telephone (216) 696-8730
Facsimile (216) 696-8731